



Practitioner's Docket No.: GR 98 P 8041

RCE/2800
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor : Thomas Huttner et al.
Applic. No. : 09/313,424 Group No. : 2823
Filed : May 17, 1999 Examiner : Brook Kebede
For : SOI Semiconductor Configuration And Method Of Fabricating The Same

Commissioner for Patents
Washington, D.C. 20231

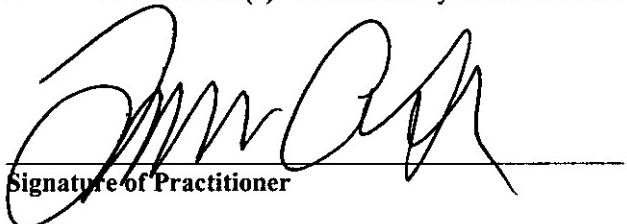
REQUEST FOR CONTINUED EXAMINATION (RCE)
(37 C.F.R. 1.114)

CERTIFICATION UNDER 37 C.F.R.1.8(a) and 1.10
(When using Express Mail, the Express Mail label number is mandatory;
Express Mail certification is optional.)

I hereby certify that, on the date shown below, this correspondence is being:

MAILING/TRANSMISSION

- deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.
- 37 C.F.R.1.8(a) - with sufficient postage as first class mail.
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- 37 C.F.R.1.8(a) - transmitted by facsimile to the Patent and Trademark Office.


Signature of Practitioner

LAURENCE A. GREENBERG
REG. NO. 29,308

Date: November 12, 2002

1. Applicant hereby requests continued examination, in accordance with 37 C.F.R. § 1.114, for the above-identified application.

TIME REQUEST IS BEING MADE

2. This request is being submitted:
 - i. Prior to abandonment of the application
 - ii. Payment of the issue fee
 - Prior to payment of the issue fee
 - Issue fee has been paid but a petition under § 1.313 has been granted
 - iii. Prior to a decision on appeal to the Board of Patent Appeals & Interferences
 - A notice is being separately sent to the Board of Patent Appeals & Interferences that this Request for Continued Examination is being filed.
 - iv. Appeal to the U.S. Court of Appeals of the Federal Circuit under 35 U.S.C. 145; or
 - Commencement of a civil action under 35 U.S.C. 146
 - Prior to the filing of such appeal or commencement of civil action
 - Such appeal or commencement of civil action has been terminated

SUBMISSION REQUIRED UNDER 37 C.F.R. § 1.114

3. a) Previously submitted
 - Consider the amendment/reply under 37 C.F.R. 1.116 previously filed on August 9, 2002.
(Any unentered amendments referred to above will be entered)
 - Consider the arguments in the Appeal Brief or Reply Brief previously submitted on
 - Other
- b) Enclosed herewith is/are:
 - An information disclosure (37 C.F.R. §1.98)
 - Form PTO-1449 (PTO/SB/08A and 08B)
 - An amendment
 - New arguments
 - New evidence in support of patentability
 - Other:

FEE FOR REQUEST (37 C.F.R. § 1.17(e))

4. This application is on behalf of:

Small entity (and status is still as small entity) \$370.00
 Large entity \$740.00

Continued Prosecution Request Fee \$740.00

FEE FOR CLAIMS

5. The fee for claims (37 C.F.R. §1.16(b)-(d) has been calculated as shown below:

	(Col.1)		(Col.2)	(Col.3)	Small Entity			Large Entity	
	Claims remaining after amendment		Highest No. previously paid for	Present Extra	Rate	Add. Fee	Or	Rate	Add. Fee
Total	16	Minus	16		x\$9=	\$		x\$18=	\$
Indep.	2	Minus	2		x\$42=	\$		x\$84=	\$
First Presentation of Multiple Dependent Claims					+\$140=	\$		+\$280=	
					Total Addit.Fee		Or	Total Addit.Fee	

(c) No additional fee is required.

or

(d) Total additional fee required is \$

EXTENSION OF TIME

6. The proceedings herein are for a patent application, and the provisions of 37 C.F.R. § 1.136(a) apply.

(a) Applicant petitions for an extension of time, the fees for which are set out in 37 C.F.R. § 1.17(a)(1)-(4), for the total number of months checked below:

Extension	Large Entity	Small Entity
one month	\$ 110.00	\$ 55.00
two months	\$ 400.00	\$ 200.00
three months	\$ 920.00	\$ 460.00
four months	\$1,440.00	\$ 720.00

Fee: \$

An extension for 1 month has already been secured, and the fee paid therefor of \$ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request \$

or

(b) Applicant believes that no extension of time is required. However, this is a conditional petition and authorization to pay the necessary fees to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

TOTAL FEE(S) DUE

7. The total fee(s) due is/are:

<input checked="" type="checkbox"/>	Continued Prosecution Fee (§ 1.17(e))	\$740.00
	Fee for additional claims (if any) (§ 1.16(b)-(d))	\$
	Extension of time fee (if any) (§ 1.17(a)(1)-(4))	\$
	Total Fee(s) Due	\$740.00

PAYMENT OF FEE(S) DUE

8. Please pay the fees for this continued examination application as follows:

<input checked="" type="checkbox"/>	Charge Credit Card the sum of	\$740.00
	(Credit Card Payment Form (PTO-2038) attached)	

Please charge any required additional fees for § 1.17(e), § 1.16(b)-(d) and/or § 1.17(a)(1)-(4) to

<input checked="" type="checkbox"/>	Account No. 12-1099 of Lerner and Greenberg, P.A.
	Credit Card (Credit Card Payment Form (PTO-2038) attached).

INVENTORSHIP

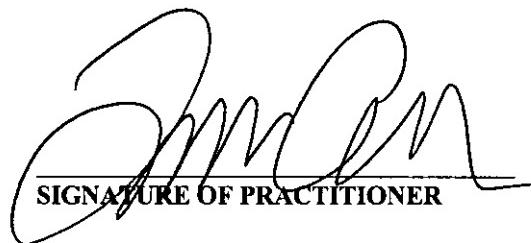
9. This application as amended names as inventors:

<input checked="" type="checkbox"/>	the same inventors as previously designated for the claims. fewer than the inventors previously designated and a statement accompanies this request for the deletion of the name or names of the person or persons who are not inventors of the invention now being claimed. a person not named previously as an inventor and a petition under 37 C.F.R. § 1.48 is/has separately: being filed been filed
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10. Instructions as to Overpayment

Credit Account No. 12-1099.

Refund



SIGNATURE OF PRACTITIONER

LAURENCE A. GREENBERG
REG. NO. 29,308

Date: November 12, 2002

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/bmb



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Thomas Huttner

RCE of Appl.: 09/313,424 filed on May 17, 1999

RCE filed : November 12, 1999

Title : SOI Semiconductor Configuration And Method Of Fabricating The Same

Examiner : Brook Kebede

Group Art Unit : 2823

P R E L I M I N A R Y A M E N D M E N T

Sir :

Responsive to the *Advisory Action* dated September 4, 2002, and in view of the attached *Request for Continued Examination* (RCE), kindly amend the above-identified application as follows:

In the Claims:

Claim 16 (amended). A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

Remarks:

Reconsideration of the application is requested.

Claims 1-6 and 16-25 remain in the application. Claim 16 has been amended. Claims 1-6 have been withdrawn from consideration.

In item 1 on page 2 of the above-identified *Advisory Action*, the Examiner stated that the proposed amendment to claim 19 correcting the claim dependency was not entered because it would raise a new issue requiring further search and consideration. In the attached *Request for Continued Examination* (RCE) the Examiner is requested to enter the amendments proposed in the previous response. These amendments will also correct the informality in the claim dependency of claim 21.

In item 4 on page 2 of the *Advisory Action*, the Examiner maintained the rejection of claims 16-20 and 24 as being obvious over by Hsu (US 5,468,657) in view of Sato et al. (US 6,121,117) under 35 U.S.C. § 103.

The detailed comments by the Examiner in the second paragraph on page 3 of the *Advisory Action* have been carefully noted by Applicants. Claim 16 has been accordingly amendment in view

of the Examiner comments. Support for the changes is found in the paragraph bridging pages 15-16 of the specification.

In view of the arguments brought forth in the previous responses, the Examiner's comments in the *Advisory Action*, and the subsequent amendment of claim 16, it is believed to be clear that *Hsu* in view of *Sato et al.* do not suggest the features of claim 16. Claim 16 is, therefore, believed to be patentable over the art and since claims 17-25 are ultimately dependent on claim 16, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 16-25 are solicited.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.



Respectfully submitted,

For Applicants

MN:cgm

November 7, 2002

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REG. NO. 29,308



Aplic. No. : 09/313,424

Version with markings to show changes made:

Claim 16 (amended). A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

[introducing] placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.